REMARKS

By this Amendment, claims 1, 7, 9, 14 and 21 are amended. Claims 5-6, 8, 10-13 and 15-20 remain in the application. Thus, claims 1 and 5-21 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

On page 2 of the Office Action, claims 1, 5-8 and 14-21 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In particular, the Examiner asserted that it was not clear from claims 1 and 14 whether the plurality of dummy patterns have the same shape, or the plurality of dummy areas have the same shape.

Claims 1 and 14 have each been amended to more clearly define that each of the plurality of dummy areas has the same shape. In view of this amendment to claims 1 and 14, the Applicant respectfully submits that claims 1 and 14, as well as claims 5-8 and 15-21 which depend therefrom, are clearly definite by particularly pointing out and distinctly claim the subject matter which the Applicant regards as the invention.

On page 3 of the Office Action, claims 1, 5-9, 14 and 19-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tamaoka et al. (U.S. Application Publication No. 2002/0014697) (hereinafter "Tamaoka").

Furthermore, on page 4 of the Office Action, claims 9-11 and 14-16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Takeuchi et al. (U.S. 6,335,560) (hereinafter "Takeuchi").

Without intending to acquiesce to these rejections, independent claims 1, 9 and 14 have each been amended to more clearly illustrate the marked differences between the present invention and the applied references. Accordingly, the Applicant respectfully submits that the present invention is patentable over the applied references for the following reasons.

The present invention provides a semiconductor device having a plurality of characteristic dummy patterns. The dummy patterns are formed in a pattern non-forming region or a non-pattern area within a same shape or having a same outline, as shown in Figures 1(A), 3(A), 4(A) and 5(A). In each shape or outline, a plurality of dummy line

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patterns (Figure 1(A)) or a single pattern with an opening (Figures 3(A), 4(A) and 5(A)) are formed.

As described in line 11 on page 2 to line 2 on page 3 of the substitute specification (line 13 on page 2 to line 5 on page 3 of the original specification), an insertion of dummy patterns reduces the global step so that a chemical mechanical polishing (CMP) of the insulating layer is thereby improved. However, an insertion of dummy patterns makes a pattern ratio large. Therefore, a disadvantage occurs with regard to an end detection of etching the pattern.

However, since each shape or outline of the dummy patterns of the present invention has a space portion (a space between the line patterns or the opening), a pattern ratio of the semiconductor device is reduced. Therefore, it is possible to more effectively suppress an increase in the global step that is formed by a deposition process (see, for example, lines 8-13 on page 9 of the substitute specification (lines 5-9 on page 10 of the original specification)).

For instance, Figure 1(A) of the present invention illustrates that each of the plurality of dummy patterns 14 has a plurality of line patterns 14a. Each of the line patterns 14a of each of the plurality of dummy patterns 14 is spaced from each other, and an area between each of the line patterns (corresponding to a slit 14b) is filled by the deposition of an insulating film (see Figure 1(B) and Figure 2(B)).

Figure 3(A) of the present invention illustrates that each of the plurality of characteristic dummy patterns 14 has the same continuous rectangular outline shape as each other and are arranged in a matrix with predetermined spacing. Furthermore, each of the rectangular-shaped dummy patterns 14 has an opening 14c.

Furthermore, Figures 4(A) and 5(A) of the present invention illustrate that each of the plurality of characteristic dummy patterns 14 has the same shape as each other, and each of the plurality of dummy patterns 14 has a space portion 14c. The space portion 14c of each of the plurality of dummy patterns 14 indicates a shape of at least one of a letter and graphic.

Independent claims 1, 9 and 14 recite the semiconductor device of the present invention as having the above-described features.

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In particular, claim 1 recites the semiconductor device of the present invention as comprising a plurality of dummy patterns, where each of the plurality of dummy patterns has a plurality of line patterns. Furthermore, each of the plurality of line patterns is spaced apart from each other by an area filled by the deposition of the insulating film.

Claim 9 recites the semiconductor device of the present invention as comprising a plurality of dummy patterns, where each of the plurality of dummy patterns has a same continuous rectangular outline shape as each other and is arranged in a matrix with predetermined spacing.

Claim 14 recites the semiconductor device of the present invention as comprising a plurality of dummy patterns being formed in a plurality of dummy areas, and that each of the plurality of dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of the semiconductor device is reduced. Furthermore, claim 14 recites that each space portion of the plurality of dummy patterns indicates a shape of at least one of a letter and graphic.

Tamaoka discloses a semiconductor device which includes a plurality of dummy patterns 30 (see Figure 1A) formed on a first insulating film 54. Each dummy pattern 30 includes a plurality of stripe-shaped patterns 30a (see Figure 1B) that are each separated from each other by a spacing 30b (see paragraph [0042]). The dummy patterns 30 shown in Figure 1B are each formed by etching a portion of the first insulating layer 54, and a portion of a pattern forming layer 53 underneath the first insulating layer 54 to result in a resist pattern 71B of dummy patterns 53b each composed of stripe-shaped portions of the first insulating layer 54b and the pattern forming layer 53b that are separated from each other by spaces 53d between adjacent stripe-shaped portions (see Figure 2D and paragraph [0048]).

Tamaoka further discloses that after the resist pattern 71B is removed, a second insulating film 57 is deposited on the semiconductor substrate 51 and the stripe-shaped portions of the dummy patterns 53b for forming air gaps. In particular, Tamaoka discloses that a second insulating film 57 is deposited to overhang like a peak on the top portions of the adjacent patterns 53b so that "an air gap can be definitely formed between the patterns [53b]." (see paragraph [0050]; emphasis added). Thereafter, a third insulating film 58 is deposited over the second insulating film 57. As a result, Tamaoka

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discloses that air gaps 73 are "formed between the fine patterns of the dummy pattern 53b so that the dummy pattern 53b can also attain the air gap structure." (see paragraph [0050] and Figures 3A-3C).

Accordingly, Tamaoka clearly discloses that an area between each fine pattern of the dummy patterns 53b are separated from each other by a space 53d that serves as an air gap 73.

In stark contrast to Tamaoka, claim 1 recites that each of the plurality of line patterns is spaced apart from each other by an area filled by the deposition of the insulating film. Tamaoka, on the other hand, discloses that each fine pattern of the dummy pattern 53b is separated from each other by an air gap 73.

Therefore, Tamaoka clearly does not disclose or suggest that each of the plurality of line patterns is spaced from each other by an area filled by the deposition of the insulating film, as recited in claim 1.

Furthermore, each fine pattern composed of each dummy pattern 53b of Tamaoka is disclosed as being separated by a space 53d that serves as the air gap 73. Therefore, Tamaoka clearly does not disclose or suggest that each of the plurality of dummy patterns has a same continuous rectangular outline shape as each other, as recited in claim 9.

Moreover, Tamaoka clearly does not disclose or suggest that each of the plurality of dummy patterns has a space portion within each of the dummy areas, where each space portion of the plurality of dummy patterns indicates a shape of at least one of a letter and graphic, as recited in claim 14.

Accordingly, Tamaoka clearly fails to disclose or suggest each and every limitation of claims 1, 9 and 14. Therefore, claims 1, 9 and 14 are clearly not anticipated by Tamaoka since Tamaoka fails to disclose each and every limitation of claims 1, 9 and 14.

Takeuchi merely discloses that one dummy pattern 7 surrounds wiring patters 7m in Figure 1. The Examiner contends that reference number 2 in Figure 16 corresponds to an "opening" in the dummy pattern 7 so that a pattern ratio of the semiconductor device is reduced. However, reference numeral 2 denotes an "active region" throughout the disclosure of Takeuchi that is unrelated to reducing a pattern ratio of the semiconductor device (see Column 4, line 43 and Column 8, lines 60-63). Furthermore, reference

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numeral 8 shown in Figure 9 of Takeuchi is disclosed as a "mark forbidden region," where a "mark" is defined as the wire patterns 7m (see Column 4, lines 47-53). Furthermore, Figures 16-18 of Takeuchi merely disclose wiring patterns 7m on the trench isolation region 1.

Accordingly, the Applicant respectfully submits that Takeuchi clearly does not disclose or suggest that each of the plurality of dummy patterns has a same continuous rectangular outline shape as each other and that each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced, as recited in claim 9.

Moreover, Takeuchi clearly does not disclose or suggest that each of the plurality of dummy patterns has a space portion within each of the dummy areas, where each space portion of the plurality of dummy patterns indicates a shape of at least one of a letter and graphic, as recited in claim 14.

In addition, Takeuchi clearly does not disclose or suggest a plurality of dummy patterns, where each of the plurality of dummy patterns has a plurality of line patterns, and each of the plurality of line patterns is spaced apart from each other by an area filled by the deposition of the insulating film, as recited in claim 1.

Accordingly, Takeuchi clearly fails to disclose or suggest each and every limitation of claims 1, 9 and 14. Therefore, claims 1, 9 and 14 are clearly not anticipated by Takeuchi since Takeuchi fails to disclose each and every limitation of claims 1, 9 and 14.

Because of the clear distinctions discussed above, it is submitted that the teachings of Tamaoka and Takeuchi clearly do not meet each and every limitation of claims 1, 9 and 14.

Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify Tamaoka and Takeuchi in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1, 9 and 14.

Therefore, it is submitted that the claims 1, 9 and 14, as well as claims 5-8, 10-13 and 15-21 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

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In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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